UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,550	09/06/2000	William A Chren, Jr.	00-LM-007	9623

30428 7590 04/14/2004

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	6

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/656,550	CHREN, JR., WILLIAM A	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Note of Reference

The Applicant is hereby requested to direct all correspondence to the undersigned Examiner, who is currently the examiner for the present application.

Drawings

This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. New corrected drawings are required. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance. Furthermore, applicant is advised to incorporate the following changes within the corrected formal drawings.

Figure 1a should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Figure 1b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected

drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

> ***The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.***
>
> ***The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.***

The abstract of the disclosure is objected to because the length exceeds the requirement of not more than 150 words. Correction is required. See MPEP § 608.01(b).

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 1, 3, 5, 6, 8-10, 12-14, 16-19 and 23-24 and original claims 2, 4, 7, 11, 15 and 20-22 filed January 12, 2004 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...neither Chren nor Arkin (prior arts of record) disclose an RNS arithmetic circuit that includes test circuitry that selectively feeds the output of an arithmetic core back to at least one of the inputs so as to induce oscillation at the output of the arithmetic core during testing, and logic circuitry that measures an oscillation frequency of the output of the arithmetic core during testing and produces a pass/fail signal to indicate whether or not the input-to-output delay of the arithmetic core is within specification based on whether the oscillation frequency is at least equal to a minimum threshold..." The Examiner disagrees. Chren teaches (title and abstract) a direct digital frequency synthesizer that employs residue number system based processors to generate output waveforms of desired frequencies. The frequency synthesizer includes a phase accumulator comprising a plurality of individual adders, each adding a predefined quantity to a digit of a frequency setting word in which the individual digits are residue digits of differing module. The outputs of the independent adders form a combined residue output word which is used to address a memory storing signal samples. In one embodiment, the memory is a dual port ROM storing samples of one-quarter of a sine wave and the dual port ROM is simultaneously addressed to read a selected sample and an associated sample corresponding to the magnitude of a sample of the sine wave advanced by 90,degree. from the first sample. A sample select logic circuit selects one of the outputs of the dual port

memory on the basis of selected bits of the combined residue word and data bits stored in the ROM with the samples to select and determine the sign of the sample of the sine wave. In another embodiment, the memory comprises a plurality of independent memories, corresponding to the number of independent adders, each storing residue information and a residue processing array processes the residue data obtained from the independent memories and provides a residue encoded signal to a residue-to-analog converter which generates the desired analog output. Furthermore, as pointed out by Chren, it is well known that analog signals of a number of different frequencies may be generated from a single source frequency by the use of analog circuits or by a combination of analog and digital circuits. In a technique known as Direct Digital Frequency Synthesis, digital data representing samples of sinusoidal wave forms of different frequencies are converted to analog sinusoidal output signals using a digital-to-analog converter. In many cases the digital data is acquired from a memory, in which are stored the values of a single cycle (or portion thereof) of a sinusoidal wave form taken at uniformly spaced intervals. The sequence of digital data points to be converted is generated by retrieval of the stored points in a uniform fashion, usually periodic. The methodology for generating the data points is well known and described in technical publications. The circuitry for selecting and retrieving the appropriate digital samples to be applied to the digital-to-analog converter is generally referred to as a numerically controlled oscillator and may be used independently of the converter. State-of-the-art numerically controlled oscillators are typically implemented in integrated circuitry. Particularly, Chren teaches (Figure 3) the outputs of the arithmetic unit that feeds the output back into the input which in turn produces an oscillation. Although Chren does not explicitly the logic circuitry to perform testing, Arkin does. Arkin

teaches (Figure 2 and col. 5, lines 10-66) the calibration data CAL is separately adjusted for each channel to calibrate out differences in delay between a state change in MCLK and a resulting state change in the test signal arriving at the DUT terminal. The edge generator produces a T1 signal pulse during each test cycle. The selected BOC signal indicates that the next test cycle begins at some point after the next MCLK pulse. The CVRN data indicates how long after that MCLK pulse that the next test cycle actually begins. The ETCA value indicates how many MCLK cycles counter 54 is to wait following the start of the next test cycle before generating a T1' pulse. The ETCB data indicates the amount of time delay circuit 56 is to delay the T1' signal in order to produce a T1 signal pulse. The adjustable delay of delay circuit 56 ranges from 0-1 MCLK period. Furthermore, Arkin teaches (col. 7, lines 20-68) a pass/fail indication upon testing as stated in the present application.

Applicant contends, "...neither Chren nor Arkin teaches or suggests a circuit or method in which oscillation is induced at the output of an arithmetic core during testing by feeding the output of the arithmetic core back to one of the inputs of the arithmetic core..." The Examiner disagrees. As stated before, Chren teaches (Figure 3) to feed back the output back into the arithmetic unit which would cause oscillations to occur, inherently. Furthermore, during testing Arkin teaches the calibration data CAL is separately adjusted for each channel to calibrate out differences in delay between a state change in MCLK and a resulting state change in the test signal arriving at the DUT terminal. The edge generator produces a T1 signal pulse during each test cycle. The selected BOC signal indicates that the next test cycle begins at some point after the next MCLK pulse. The CVRN data indicates how long after that MCLK pulse that the next test cycle actually begins. The ETCA value indicates how many MCLK cycles counter 54 is to

wait following the start of the next test cycle before generating a T1' pulse. The ETCB data indicates the amount of time delay circuit 56 is to delay the T1' signal in order to produce a T1 signal pulse. The adjustable delay of delay circuit 56 ranges from 0-1 MCLK period.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chren (USPN 5430764) in view of Arkin (USPN 5917834) further in view of prior art admissions. See office action, paper No. 3.

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 1, 3, 5, 6, 8-10, 12-14, 16-19 and 23-24 and original claims 2, 4, 7, 11, 15 and 20-22. All arguments have been considered. It is the Examiner's conclusion that amended claims 1, 3, 5, 6, 8-10, 12-14, 16-19 and 23-24 and original claims 2, 4, 7, 11, 15 and 20-22 are not patentably distinct or non-obvious over the prior art of record. See office action, paper No. 3.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
April 6, 2004

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100